Notice of Allowability	Application No.	Applicant(s)	
	10/815,288	NEFIAN ET AL.	
	Examiner	Art Unit	
	Chuck O. Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/23/07*.

2. ☒ The allowed claim(s) is/are *1,2, 4, 7, 9 - 12, 15, 17 - 21, 23 - 26 (renumbered as 1 - 18)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *07/06/07* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TUAN DAM
SUPERVISORY PATENT EXAMINER

Examiners Amendment

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Steven Laut registration no. 47,736 on July 06 2007, to obviate any potential 101 issues.

The proposed amendment dated 07/06/07 has received accepted and adopted by the Examiner-see attachment herein.

The application has been amended as follows:

IN THE CLAIMS

2. Please amend claims 1, 7, 15 and 21 as attached herein see pages 5 - 9.

Claim 7 (currently amended)

On line 1, after " comprising ", delete [a machine readable medium] and insert a storage device

See attached document as proposed by Applicant to amend claims

Reasons for Allowance

3. Examiner has reviewed and considered Applicants arguments and per Applicants current amendment of claims of 04/23/07 as well as Applicants arguments on pages 8 – 10, claims 1, 2, 4, 7, 9 –12, 15,17 – 21 and 23 – 26 are now in condition for allowance.

The following is an Examiner's statement of reasons for allowance.

The prior art of record does not teach or fairly suggest at least the limitations of:

"...determining a distance with between centers of at least two consecutive histogram bins, comparing the distance with said selected threshold value...using the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment", and as best illustrated by figs 1, in such a manner as recited in independent claims 1, 7, 15 and 21.

Therefore, all claims 1, 2, 4, 7, 9 –12, 15,17 – 21 and 23 – 26 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Correspondence Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-2723698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-2723695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUAN DAM
SUPERVISORY PATENT EXAMINER

Claim 1 (Currently Amended) A method of determining where compiler optimization can be implemented comprising:

selecting a phase threshold value,

receiving a plurality of branch trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses,

determining a plurality of branch address vectors from the plurality of branch addresses,

determining histogram bins ~~from~~ for the plurality of branch address vectors,

determining a distance between centers of at least two consecutive histogram bins,

comparing the distance with said selected threshold value,

determining major execution phases of an executable process based on the comparison, and

using the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Claim 2 (Previously Presented) The method of claim 1, said plurality of trace buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 3 (Canceled)

Claim 4 (Previously Presented) The method of claim 1, where a result of said determining major execution phases is used for dynamically compiling executable code to optimize said executable code.

Claims 5-6 (Canceled)

Claim 7 (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed cause a machine to:

select a phase threshold value,

receive a plurality of branch trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses,

determine a plurality of branch address vectors from the plurality of branch addresses,

determine histogram bins ~~from~~ for the plurality of branch address vectors,

determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping,

compare the distance with said selected threshold value,

determine major execution phases of an executable process based on a result of the compare, and

use the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Claim 8 (Canceled)

Claim 9 (Previously Presented) The apparatus of claim 8, wherein said determine major execution phases is dynamic at a predetermined periodic rate.

Claim 10 (Previously Presented) The apparatus of claim 8, wherein said determine major execution phases is manually commenced.

Claim 11 (Previously Presented) The apparatus of claim 7, said plurality of branch trace buffers in sequence comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 12 (Previously Presented) The apparatus of claim 7, where a result of said determine major execution phases instruction is used for dynamically compiling executable code to optimize said executable code.

Claims 13-14 (Canceled)

Claim 15 (Currently Amended) A system comprising:

a processor coupled to one of a main memory and a cache memory,

at least one process to communicate with said memory, and

a phase detector that operates to determine major execution phases of said at least one process and to comparing a distance between centers of at least two consecutive histogram bins for a plurality of branch address vectors determined from a plurality of branch addresses with a threshold value to determine where compiler optimization is needed to improve performance of the at least one process in a managed run-time environment.

Claim 16 (Canceled)

Claim 17 (Canceled)

Claim 18 (Currently Amended) The system of claim 17, said phase detector having logic to:

determine ~~a~~ the plurality of consecutive branch addresses representing a branch trace buffer,

determine a stable phase histogram for a plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

Claim 19 (Original) The system of claim 15, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

Claim 20 (Original) The system of claim 17, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 21 (Currently Amended) A system comprising:

a first device having a first processor coupled to a first memory and at least one process to communicate with said first memory, and

a second device having a second processor coupled to a second memory and at least another process to communicate with said second memory,

wherein a phase detector process operating in one of said first processor and said second processor operates to compare a distance between centers of at least two consecutive histogram bins for a plurality of branch address vectors determined from a plurality of branch addresses with a threshold value to determine major execution phases of one of said one process and said another process within one of said first device and said second device for determining where compiler optimization is needed for one of said one process and said another process to improve performance in a managed run-time environment.

Claim 22 (Canceled)

Claim 23 (Currently Amended) The system of claim 21, said phase detector having logic to:

receive a plurality of trace buffers in sequence, the plurality of trace buffers including a plurality of branch addresses,

determine ~~a~~ the plurality of branch address vectors,

determine the histogram bins ~~from~~ for the plurality of branch address vectors,

determine ~~a~~ the distance between centers of the at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

compare the distance with ~~a~~ the predetermined threshold value.

Claim 24 (Currently Amended) The system of claim 23, said phase detector having logic to:

determine a plurality of consecutive branch addresses representing a branch trace buffer,

determine a stable phase histogram for the plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

Claim 25 (Original) The system of claim 21, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

Claim 26 (Original) The system of claim 23, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.